SELF ALIGNED DAMASCENE GATE

FIELD OF THE INVENTION

[0001] The present invention relates generally to semiconductor devices and, more particularly, to metal-oxide semiconductor field-effect transistor (MOSFET) devices with a self aligned damascene gate and methods of making these devices.

BACKGROUND OF THE INVENTION

[0002] Scaling of device dimensions has been a primary factor driving improvements in integrated circuit performance and reduction in integrated circuit cost. Due to limitations associated with gate-oxide thicknesses and source/drain (S/D) junction depths, scaling of existing bulk MOSFET devices below the 0.1 μm process generation may be difficult, if not impossible. New device structures and new materials, thus, are likely to be needed to improve FET performance.

[0003] Double-gate MOSFETs represent devices that are candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, the use of two gates to control the channel significantly suppresses short-channel effects. A FinFET is a double-gate structure that includes a channel formed in a vertical fin. Although a double-gate structure, the FinFET is similar to existing planar MOSFETs in layout and fabrication techniques. The FinFET also provides a range of channel lengths, CMOS compatibility, and large packing density compared to other double-gate structures.

SUMMARY OF THE INVENTION

[0004] Implementations consistent with the principles of the invention provide FinFET devices that include a damascene gate formed with a self aligned gate mask and methods for manufacturing these devices.

[0005] In one aspect consistent with the principles of the invention, a method for forming a metal-oxide semiconductor field-effect transistor (MOSFET) includes patterning a fin area, a source region, and a drain region on a substrate, forming a fin in the fin area, and forming a mask in the fin area. The method further includes etching the mask to expose a channel area of the MOSFET, etching the fin to thin a width of the fin in the channel area, forming a gate over the fin, and forming contacts to the gate, the source region, and the drain region.

[0006] In another aspect consistent with the principles of the invention, a method for forming a MOSFET includes forming a fin on a substrate; forming a mask on the substrate; etching the mask to expose a channel area of the MOSFET; thinning a width of the fin in the channel area; and forming a gate over the fin, where the gate extends on each side of the fin.

[0007] In yet another aspect consistent with the principles of the invention, a MOSFET includes a fin having a width of approximately 100 Å to 400 Å formed on a substrate, a gate dielectric formed on side surfaces of the fin, and a gate electrode formed covering the fin.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, explain the invention. In the drawings,

[0009] Fig. 1 illustrates an exemplary process for fabricating a MOSFET in accordance with an implementation consistent with the principles of the invention;

[0010] Figs. 2A-6C illustrate exemplary top and cross-sectional views of a MOSFET fabricated according to the processing described in Fig. 1;

[0011] Figs. 7A-7C illustrate a process for forming spacers according to another implementation consistent with the principles of the invention;

[0012] Figs. 8A-8C illustrate an exemplary process for removing fin sidewall damage; and

[0013] Fig. 9 illustrates an exemplary process for improving mobility of a FinFET device.

DETAILED DESCRIPTION

[0014] The following detailed description of implementations consistent with the present invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

[0015] Implementations consistent with the principles of the invention provide FinFET devices that include a self aligned damascene gate and methods for manufacturing these devices. Such FinFET devices have certain advantages. For example, only the active area of the fin is at the minimum channel length, which reduces source/drain resistance. The gate is also self aligned to the minimum channel area, which significantly reduces the parasitic source/drain resistance of the device. In traditional FinFET approaches, the narrow channel is

usually significantly longer than the gate length in order to account for gate-to-fin overlay tolerance. Also, the gate patterning is done on a planar substrate (e.g., a polished damascene material), which provides increased lithography margin since the depth of focus of aggressive lithography schemes tends to be quite low. Also, critical dimension variation due to changes in resist thickness over topography (i.e., CD swing0 can be avoided since the resist coating is on a planarized surface.

EXEMPLARY MOSFET

[0016] Fig. 1 illustrates an exemplary process for fabricating a MOSFET in accordance with an implementation consistent with the principles of the invention. Figs. 2A-6C illustrate exemplary top and cross-sectional views of a MOSFET fabricated according to the processing described with regard to Fig. 1.

[0017] With reference to Figs. 1 and 2A-2C, processing may begin with semiconductor device 200. As shown in the cross-sectional views in Figs. 2A and 2B, semiconductor device 200 may include a silicon on insulator (SOI) structure that includes a silicon (Si) substrate 210, a buried oxide layer 220, and a silicon layer 230 on the buried oxide layer 220. Buried oxide layer 220 and silicon layer 230 may be formed on substrate 210 in a conventional manner. The thickness of buried oxide layer 220 may range, for example, from about 1,000 Å to 10,000 Å. The thickness of silicon layer 230 may range, for example, from about 400 Å to 1,500 Å. The silicon thickness may be as thick as possible since increased thickness leads to enhanced width of the device (i.e., more current flow along the sidewall of the fin and thereby higher drive current (in a MOSFET $I \propto W/L$)). Usually it is difficult to use a thick

silicon thickness in a conventional FinFET approach since that also leads to a bigger step in the gate lithography step and poor lithography margin.

[0018] It will be appreciated that silicon layer 230 is used to form the fin. In alternative implementations, substrate 210 and layer 230 may include other semiconductor materials, such as germanium, or combinations of semiconductor materials, such as silicon-germanium. Buried oxide layer 220 may include a silicon oxide or other types of dielectric materials.

[0019] A silicon nitride, or another type of material, may be formed on silicon layer 230 and may function as a bottom antireflective coating (BARC) 240 for subsequent processing, as illustrated in Figs. 2A and 2B. The thickness of BARC layer 240 may range from approximately 150 Å to 350 Å. A photoresist 250, or the like, may be deposited and patterned to facilitate formation of a large fin area and the source and drain regions (act 110), as shown in Figs. 2A-2C. Photoresist 250 may be deposited to a thickness ranging from about 1,000 Å to 4,000 Å. Fig. 2C illustrates the top view of semiconductor device 200 of Figs. 2A and 2B. The cross-section in Fig. 2A is taken along line X in Fig. 2C and the cross-section in Fig. 2B is taken along line Y in Fig. 2C.

[0020] Silicon layer 230 may be etched to form a fin 310 (act 120), as shown in Figs. 3A and 3B. For example, the portion of silicon layer 230 not located under photoresist 250 may be etched with the etching terminating on buried oxide layer 220. Photoresist 250 may then be removed. The width of fin 310, as shown in Fig. 3B, may range from approximately 500 Å to 800 Å.

[0021] A damascene mask may be formed in the area of fin 310 (act 130), as illustrated in Figs. 3A-3C. For example, a damascene material 320, such as silicon oxide, silicon nitride,

SiCOH, etc., may be deposited over semiconductor device 200 to a thickness ranging from approximately 800 Å to 2,200 Å (to enclose fin 310 and BARC 240) and then polished using known techniques, as illustrated in Figs. 3A and 3B. Damascene material 320 may function as a BARC for subsequent processing. Damascene material 320 may then be etched using a gate mask to expose a channel area 330 in the gate opening, as shown in Figs. 3A-3C. The width of channel area 330, as illustrated in Fig. 3C, may range from approximately 300 Å to 500 Å. The gate mask used to expose channel area 330 may be created using aggressive lithography and patterning techniques known to those skilled in the art.

[0022] The width of fin 310 may then be reduced (act 140), as illustrated in Figs. 4A-4C. One or more etching techniques may be used to laterally etch fin 310 in channel area 330. For example, a thermal oxidation of Si followed by a dilute HF dip may be used. Other types of etches may alternatively to be used. For example, Si may be etched in a downstream F plasma where the chemical selectivity of the Si etch in F species over oxide is very high, or a lateral Si etch in HBr based plasma chemistries may be used.

[0023] The amount of silicon removed may range from approximately 100 Å to 200 Å per side, as illustrated in Fig. 4B. The resulting width of fin 310 may range from approximately 100 Å to 400 Å. BARC 240 may remain in implementations consistent with the principles of the invention, as illustrated in Fig. 4B. In other implementations, BARC 240 may be removed. Fig. 4C illustrates a top view of semiconductor device 200 after fin 310 has been thinned in channel area 330.

[0024] A gate may then be formed (act 150), as illustrated in Figs. 5A-5C. For example, a gate dielectric material 510 may be deposited or thermally grown on the side surfaces of fin

310 using known techniques, as illustrated in Fig. 5B. Gate dielectric material 510 may include conventional dielectric materials, such as an oxide (e.g., silicon dioxide), silicon oxy-nitride, or high dielectric constant (high K) materials, such as HfO_2. In other implementations, a silicon nitride or other materials may be used to form the gate dielectric. Gate dielectric material 510 may be formed at a thickness ranging from approximately 10 Å to 20 Å.

[0025] A gate electrode material 520 may then be deposited over semiconductor device 200 and polished, as illustrated in Figs. 5A and 5B. Gate electrode material 520 may be polished (e.g., via chemical-mechanical polishing (CMP)) to remove any gate material over damascene material 320, as illustrated in Figs. 5A and 5B. A number of materials may be used for gate electrode material 520. For example, gate electrode material 520 may include a polycrystalline silicon or other types of conductive material, such as germanium or combinations of silicon and germanium, or metals, such as W, WN, TaN, TiN, etc. Gate electrode material 520 may be formed at a thickness ranging from approximately 700 Å to 2,100 Å, as illustrated in Fig. 5B, which may be approximately equal to the thickness of damascene material 320 (some of which may be lost due to the polishing). Fig. 5C illustrates a top view of semiconductor 200 after gate electrode 520 is formed. The dotted lines in Fig. 5C represent the thinned portion of fin 310. Gate dielectric layer 510 is not illustrated in Fig. 5C for simplicity.

[0026] Source, drain, and gate contacts may then be formed (act 160), as illustrated in Figs. 6A-6C. For example in one implementation, large contact areas may be opened over fin 310 on either side of the gate, as illustrated in Fig. 6A. Source and drain contact areas 610

and 620 may be opened by etching through the extra amount of damascene material 320 left above fin 310 and also removing BARC 240. Gate contact area 630 may also be formed on gate electrode 520. It may be possible for these contact areas 610-630 to be larger than the actual dimensions of fin 310 and the source/drain.

[0027] Silicidation, such as $CoSi_2$ or NiSi silicidation, can then occur in these openings. The $CoSi_2$ or NiSi silicidation occurs only where there is polysilicon (i.e., gate) or silicon (i.e., source/drain) and whatever fin region (wide fin) is exposed. The unreacted cobalt or nickel (wherever there is no silicon) can be etched away just as is done in typical self-aligned silicide schemes in use by the industry today.

[0028] In another implementation, damascene material 320 and BARC 240 may be removed from the top of fin 310 and the source/drain. Then, a sidewall spacer may be formed on the sides of the gate and fin 310. Next, a silicide metal, such as cobalt or nickel, may be deposited to form a self aligned silicide wherever there is silicon or polysilicon exposed at the top (i.e., on the gate and on the exposed fin channel).

[0029] The resulting semiconductor device 200, therefore, may include a self aligned damascene gate formed on either side of fin 310. Fin 310 is thinned in the channel area, as illustrated by the dotted lines in Fig. 6C.

[0030] According to another implementation consistent with the principles of the invention, spacers may be formed for the transfer of the damascene gate to make the gate length smaller. Figs. 7A-7C illustrate an exemplary process for forming spacers according to an alternate implementation consistent with the principles of the invention. As illustrated in Figs. 7A-7C, a hardmask 710 may be opened (Fig. 7A), spacers 720 may be formed (Fig. 7B),

and the transfer of the damascene gate may be performed in the opening (Fig. 7C). The spacer formation inside the damascene gate opening may facilitate printing of small spaces (as mentioned above) in order to form small gate length devices. The spacer technique enables the formation of smaller spaces than may be attained by photolithographic shrinking alone.

[0031] In another implementation, damascene gate shrink techniques, such as the ones described in copending, commonly assigned applications entitled, "FINFET GATE FORMATION USING REVERSE TRIM AND OXIDE POLISH" (Serial No. 10/459,589) (Docket No. H1122), filed June 12, 2003, "FINFET GATE FORMATION USING REVERSE TRIM OF DUMMY GATE" (Serial No. 10/320,536) (Docket No. H1121), filed December 17, 2002, and "ETCH STOP LAYER FOR ETCHING FINFET GATE OVER A LARGE TOPOGRAPHY" (Serial No. 10/632,989) (Docket No. H1172), filed August 4, 2003, which are incorporated herein by reference.

[0032] In yet another implementation, a metal gate electrode may be used instead of the polysilicon damascene process described above.

OTHER IMPLEMENTATIONS

[0033] There is a need in the art to remove damage that may occur to the side surfaces (i.e., sidewalls) of a fin during processing. Figs. 8A-8C illustrate an exemplary process for removing fin sidewall damage. A semiconductor device 800 may include a fin layer 810 and a cover layer 820 formed on a substrate 830, as illustrated in Fig. 8A. Fin layer 810 may include a semiconductor material, such as silicon or germanium, or combinations of semiconductor materials. Cover layer 820 may, for example, include a silicon nitride material

or some other type of material capable of protecting fin layer 810 during the fabrication process.

[0034] Fin layer 810 and cover layer 820 may be etched using a conventional dry etching technique to form fin 840, as illustrated in Fig. 8B. A conventional wet etching technique may then be used to remove fin sidewall damage, as illustrated in Fig. 8C. During the wet etching, the width of fin 840 may be thinned by approximately 20 Å to 40 Å per side. Wet etching of silicon may also result in some buried oxide loss since it is difficult when wet etching to get good selectivity of silicon to silicon dioxide.

[0035] There is also a need in the art to improve the mobility of a FinFET device. Fig. 9 illustrates an exemplary process for improving mobility of a FinFET device. A die-attach material may be formed on a package, as illustrated in Fig. 9. The die-attach material may be selected to induce stress (strain) in the FinFET channel. A die may then be attached to the die-attach material, as illustrated in Fig. 9. Tensile stress induced in the silicon FinFET channel may result in enhanced hole mobility, which can help significantly improve PMOS FinFET performance. The die-attach material and process may be such that the residual stress in the silicon layer is tensile. For example, if the package material did not shrink as fast as the silicon layer after the (hot) die attach/solder/bump process, then the silicon layer could be in tensile stress when cooled to lower temperatures.

CONCLUSION

[0036] Implementations consistent with the principles of the invention provide FinFET devices that include a damascene gate formed with a self aligned gate mask and methods for manufacturing these devices. These FinFET devices have certain advantages. For example,

only the active area of the fin is at the minimum channel length, the gate is self aligned to the minimum channel, and the gate patterning is performed on a planar substrate (e.g., a polished damascene material).

[0037] The foregoing description of exemplary embodiments of the present invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention.

[0038] For example, in the above descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of implementations consistent with the present invention. These implementations and other implementations can be practiced, however, without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional deposition, photolithographic and etching techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

[0039] While a series of acts has been described with regard to Fig. 1, the order of the acts may be varied in other implementations consistent with the present invention. Moreover, non-dependent acts may be implemented in parallel.

[0040] No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where

only one item is intended, the term "one" or similar language is used. The scope of the invention is defined by the claims and their equivalents.